UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/709,325  | 04/28/2004  | Kenneth L. DeVries   | BUR920030184US1     | 3324             |
| 48148 7590 08/08/2007 MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC 8321 OLD COURTHOUSE ROAD |             |                      | EXAMINER            |                  |
|   |             |                      | IM, JUNGHWA M       |                  |
| SUITE 200<br>VIENNA, VA 22182-3817  |             |                      | ART UNIT            | PAPER NUMBER     |
| •   |             |                      | 2811                |                  |
|   |             |                      |                     | DEL HADDA VODA   |
|   |             |                      | MAIL DATE           | DELIVERY MODE    |
|   |             |                      | 08/08/2007          | PAPER            |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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| APPLICATION NO./<br>CONTROL NO. | FILING DATE | FIRST NAMED INVENTOR / PATENT IN REEXAMINATION | ATTORNEY DOCKET NO. |
|---------------------------------|-------------|--|---------------------|
| 10709325                        | 4/28/04     | DEVRIES ET AL.                                 | BUR920030184US1     |

MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817 Junghwa M.. Im

ART UNIT PAPER

2811

20070805

DATE MAILED:

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## **Commissioner for Patents**

The reply brief filed July 5, 2007 has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Junghwa M. Im Examiner

Art Unit 2811

jmi

Appellants' Reply Brief on Appeal

S/N: 10/709,325 (BUR.107)

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

DeVries, et al.

Serial No.: S/N: 10/709,325 Group Art Unit: 2811

Filed: April 28, 2004 Examiner: Im, J. M.

For: METHOD AND STRUCTURE FOR CONNECTING GROUND/POWER

NETWORKS TO PREVENT CHARGE DAMAGE IN SILICON ON

INSULATOR

Commissioner of Patents Alexandria, VA 22313-1450 noted 8/5/2007

## **APPELLANTS' REPLY BRIEF ON APPEAL**

Sir:

Appellants respectfully reply herein to the Examiner's Answer mailed on April 4, 2007, in the above-identified application.

Appellants respectfully submit that there are at least five fundamental flaws in the Examiner's position presented in the Examiner's Answer, as follows.

- 1. Even if all three references of record were to be combined, the combination would not result in the present invention described by the claims;
- 2. The Examiner's position fails to honor the terminology (e.g., "circuit design modules") used in the claims, as this terminology is defined in the specification;
  - 3. The Examiner's position improperly ignores structural terminology (e.g., "grids of

S/N: 10/709,325 (BUR920030184US1)